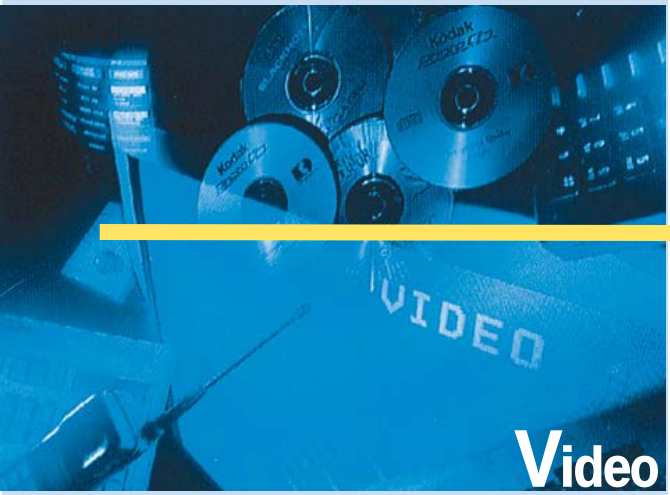



VITEC MULTIMEDIA PRODUCTS TECHNOLOGY

DIGITAL VIDEO EXPERTS

www.vitecmm.com

# VP³-PMC™

## Video Parallel Programmable Processor

## *Multi DSP Platform* for OEMs & Developers

**VP³-PMC™** is an extremely powerful parallel programmable processing platform dedicated to professional and industrial video applications such as :

- AVC / H.264 real time top quality encoders,
- MPEG-2 to AVC / H.264 transcoders,
- Real time content analysis,
- Image processing, ...

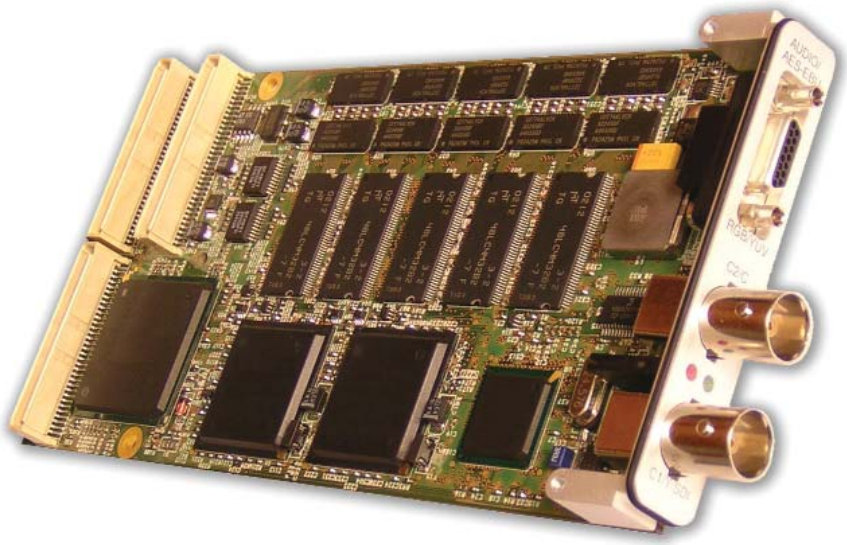
The VP³-PMC™ board has a standardized "PMC" form factor. A PMC mezzanine card can be used in conjunction with carrier boards compliant to :

- CompactPCI,
- Standard PCI,
- VME, ...

Therefore the VP³-PMC™ card can be used in numerous application contexts.

### *Key features :*

- **24 GIPS and more,**
- **5 x TMS320DM642™ DSPs,**
- **Hardware coprocessor,**
- **Digital Video input (SDI : SMPTE 259M-C),**
- **Analog Video inputs (YUV, RGBS, S-Video, composite),**
- **Digital Audio input (AES/EBU),**
- **Analog Audio inputs (balanced & unbalanced),**
- **Audio and Video sync,**
- **Audio de-embedding,**
- **DVB-ASI compliant,**
- **PCI interface.**



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Specifications subject to change without prior notice - Sept 2004

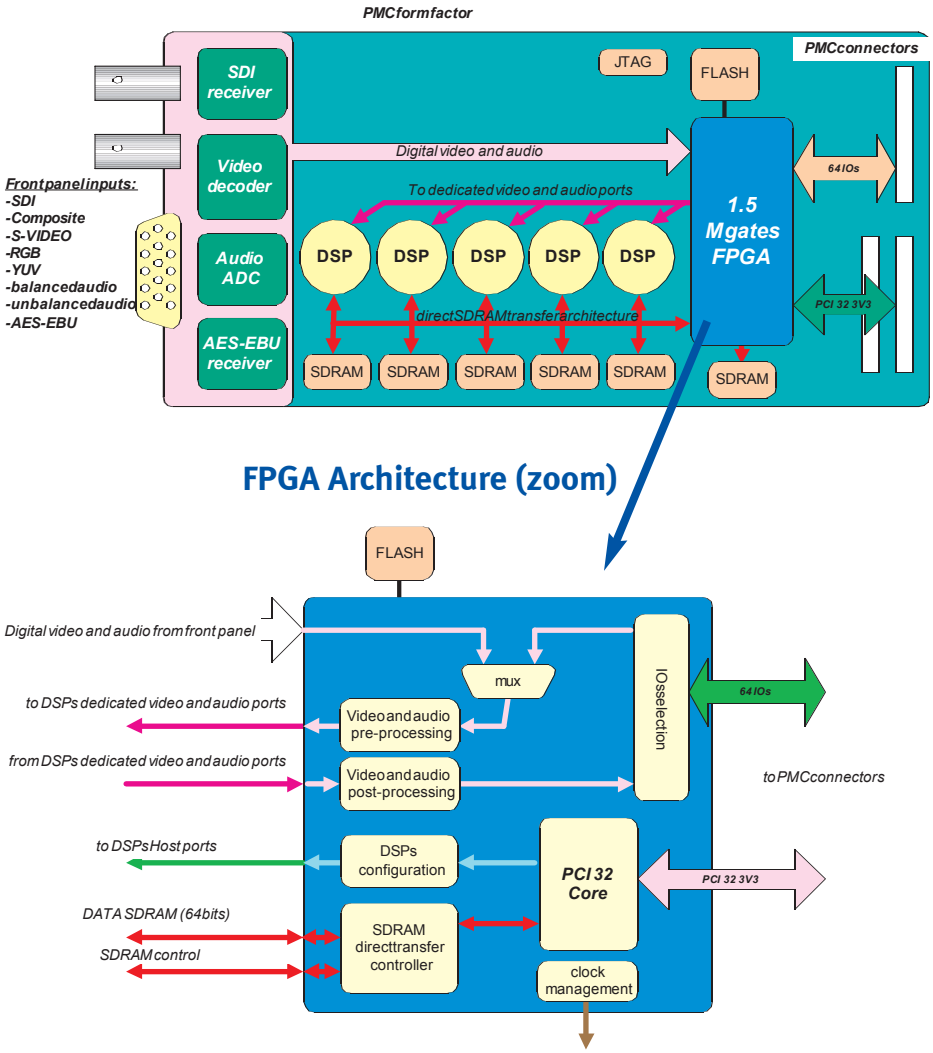
# ARCHITECTURE OF THE BOARD

**VP³-PMC™** implements 5 x TMS320DM642™ DSPs from Texas Instruments running at 600 MHz or more (and soon 720 MHz) thus providing up to **24 GIPS** with a maximum of 4 operations per instruction (4 operations of 8 bits, 2 operations of 16 bits or 1 operation of 32 bits) thus leading to a maximum of **96 GOPS**.

Each DSP has a private local memory of 32 MB (SDRAM running at 100 MHz and 64 bits, which provides a throughput of 800 MB/s).

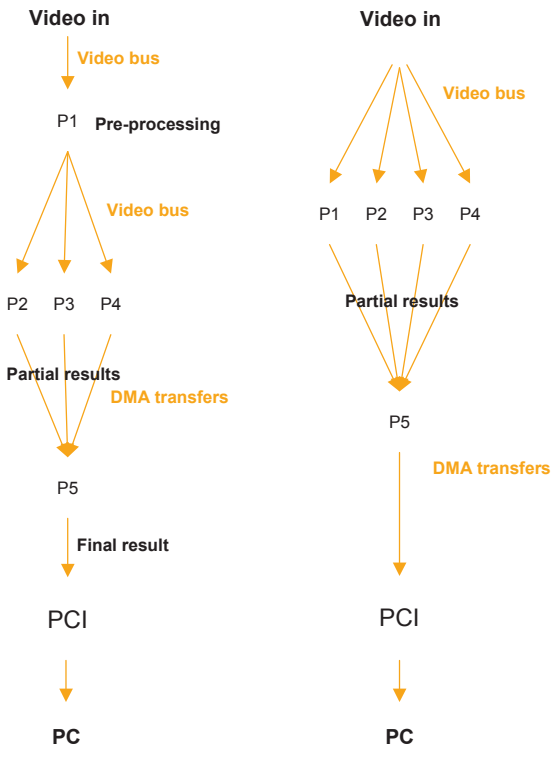
The board has a 3V3 PCI interface rev 2.3. It also offers a JN4 connector with 64 IOs signals which can be configured by software to fit with any pin-out requested by the carrier board.

## Architecture overview




# CONFIGURABLE TOPOLOGY

**VP³-PMC™** architecture is highly flexible and can be configured to fit to the specific needs of the developer's applications. Any DSP can capture video and audio through the video bus (simultaneously or not). The topology of the array of processors can be defined as a simple pipeline of five processors, a fully parallel scheme or a mix of both.



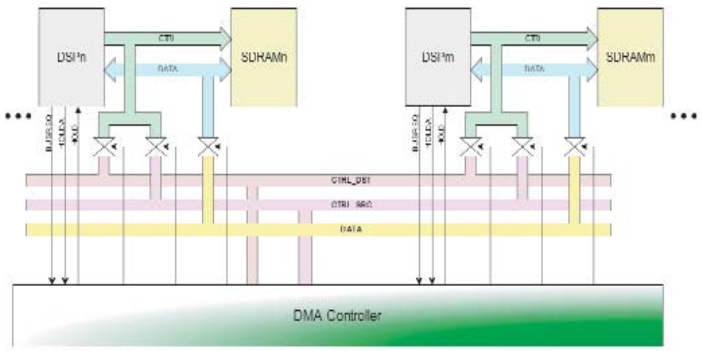
## INTER-DSPs COMMUNICATION

DSPs can communicate information to each others in several ways :

- Direct memory to memory block exchanges through the DMA controller services. High performance DMA inter-processor's communication channels have been optimized to allow 1 to 1, 1 to n or 1 to all data exchanges.
- The host busses of the DSPs are linked to PCI interface and can send/receive messages to/from the host through the PCI interface.

## DMA CONTROLLER PRINCIPLE

One DSP initiates a Memory Block Transfer by sending a request to the DMA Controller specifying the list of destination DSPs which shall receive the message. The hardware controller puts the source and destination DSPs in hold state and takes control of their local memories to read the source memory and write into all the destination memories simultaneously. Once the transfer is achieved the DMA controller sends an interrupt to the source DSP to warn it that its message has been sent and also to the destination DSPs to warn them that they received a message.




The DMA controller also supports data transfers from DSP memory to the host through the PCI interface and vice-versa.

## HARDWARE COPROCESSORS

**VP³-PMC^tm** includes a very powerful FPGA which has an overall capacity of 1.5 Million gates in 90 nm technology. Vitec is using part of this component to implement some basic functions like PCI interface, DMA transfers Controller and IOs interfaces. A little bit more than 1 Million gates stays available for user-defined hardware co-processors which communicate with the DSPs using DMA transfers. For example, customers may implement a CABAC co-processor, an image preprocessing module or even a motion estimation processor. There is an SDRAM of 16 Mbytes directly connected to the FPGA and available for a user application. The content of the FPGA can be downloaded at initialization of the board from the flash memory which can be itself reprogrammed by software.

## SOFTWARE TOOLS

**VP³-PMC^tm** comes with a complete software environment :

- Windows WDM driver (.SYS),
- The source code of a sample application running under Windows XP/2000 and addressing directly the WDM driver,
- Source code of DSP sample applications such as :
  - video capture,
  - audio capture,
  - memory BIST,
  - DMA transfers.
- Vitec recommends the use of the Texas Instruments development tools to develop software for the DSPs themselves,
  - C/C++ compiler,
  - simulator,
  - emulator via the RTDS protocol and standard JTAG connector,
- Multi-DSP applications can be emulated by instancing several times the TI emulator software under Windows and the JTAG connector on the **VP³** board.

Remark : the **VP³-PMC^tm** and the **VP³** platforms have an identical DMA architecture and mainly differ by the IOs. Therefore, one can, for instance, develop software with **VP³** and then port it with very little modifications to the **VP³-PMC^tm** platform.

# SOFTWARE TOOLS

A complete framework, called LiveWire™, for developers who want to use **VP³-PMC^tm** hardware to develop a product running under Windows. LiveWire™ provides a set of ready to use connectable components leading to a drastic cut of the development time. LiveWire™ has many advantages. It :

- ensures highly flexible, scalable, truly customizable solutions,
- is designed to allow well-structured parallel development,
- allows to concentrate on solution specific tasks,
- overcomes the limitations of existing technologies such as DirectShow and COM in general,
- allows live reconnection of functional components without interruption of active processes,
- is compatible with Win32, COM, scriptable languages (Visual Basic, Java Script,...),
- takes advantages of XML based technologies and uses the Apache Xerces XML parser,
- provides different levels of SDK abstraction, from high level API for scripting languages through Win32 API for limited backward compatibility to the low level set of COM Interfaces for advanced development in C++.

LiveWire™ parts :
- LiveWire Core
- LiveWire Components
- LiveWire XML-based Profiles
- LiveWire Custom Components Wizard for MS Visual Studio C++
- LiveWire Multiplatform Shell
- LiveWire SDK
- LiveWire Tutorial and Samples

To start using LiveWire™ based products, all what has to be done is to create an instance of Assembly Container, initialize it with XML-based Configuration Profile and run. It all can be done in less than a dozen lines of code. Different sophisticated profiles can be created without any programming at all, using Integrated Property Page or directly by editing the XML file in the text editor of your choice. And components parameters persistence comes along for free.

To use advanced features, such as Command Scheduling and Atomic Command Blocks, just a little programming will be needed. With a few extra lines of code you can complete an application capable of running execution scripts with frame accurate precision.

Custom LiveWire™ components creation is simplified by Wizard and they can be easily integrated into existing Assemblies.

Probably most important advantage shown here is layered structure of the Live Wire™ framework. It allows to start quick and go into details only as deep as necessary, avoiding steep learning curve of new technology.

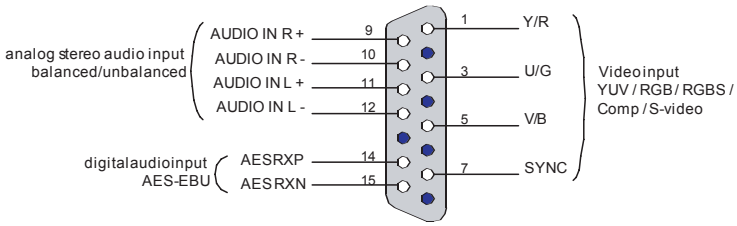
# TECHNICAL SPECIFICATIONS

| | | |
|---|---|---|
| **Inputs** | **Video Inputs** | SDI, YUV, RGB, S-Video, NTSC, PAL, SECAM |
| | **Audio Inputs** | AES/EBU, Audio de-embedding from SDI, analog balanced and unbalanced stereo |

| | |
|---|---|
| **Other interfaces** | **DVB-ASI input** |
| | **The PCI interface is a 32 bits 33MHz PCI rev2.3 3V3 only** |
| | **64 pin configurable IO connector (JN4)** |
| | **14-pin JTAG for external emulation hardware support. This is used to connect VP³-PMC to the TI emulator software** |

| | |
|---|---|
| **Other specs** | **VP³-PMC has a standard PMC size : 149 mm x 74 mm (5.87" x 2.91" inch)** |
| | **VP³-PMC power consumption is 14,5 W max and 10,4 W in average** |
| | **VP³-PMC weight is 123 g** |
| | **The capacity of the Flash Memory is 8 MB** |

***micro DB-15 connector pinout***




# DSPs SPECIFICATIONS

**VP³-PMC^tm** uses 5 DSP DM642 :

- **High-Performance Digital Media Processor :**
  - 600-MHz Clock Rate (and soon 720 MHz),
  - Eight 32-Bit Instructions/Cycle,
  - 4800 MIPS,
  - Fully Software-Compatible With C64x.
- **VelociTI.2. Extensions to VelociTI. Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x. DSP Core :**
  - Eight Highly Independent Functional Units With VelociTI.2. Extensions:
  - Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle,
  - Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle,
  - Load-Store Architecture With Non-Aligned Support,
  - 64 32-Bit General-Purpose Registers,
  - Instruction Packing Reduces Code Size,
  - All Instructions Conditional.
- **Instruction Set Features**
  - Byte-Addressable (8-/16-/32-/64-Bit Data),
  - 8-Bit Overflow Protection,
  - Bit-Field Extract, Set, Clear,
  - Normalization, Saturation, Bit-Counting,
  - VelociTI.2. Increased Orthogonality.
- **L1/L2 Memory Architecture**
  - 128K-Bit (16K-Byte) L1P Program Cache (Direct Mapped),
  - 128K-Bit (16K-Byte) L1D Data Cache (2-Way Set-Associative),
  - 2M-Bit (256K-Byte) L2 Unified Mapped RAM/Cache (Flexible RAM/Cache Allocation).
- **Endianess: Little Endian**
- **Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)**
- **10/100 Mb/s Ethernet MAC (EMAC)**
- **Three Configurable Video Ports :** supports Multiple Resolutions and Video Standards
- **Three 32-Bit General-Purpose Timers**
- **IEEE-1149.1 (JTAG†)**

C64x, VelociTI.2, VelociTI, and TMS320C64x are trademarks of Texas Instruments.
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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.