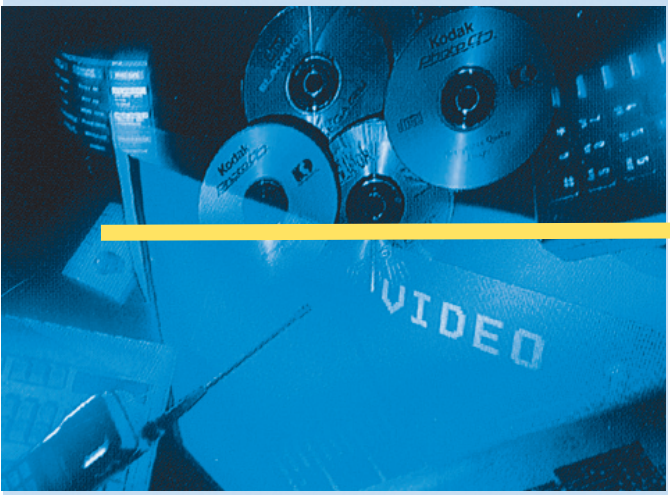


PRODUCTS
VITEC MULTIMEDIA
TECHNOLOGY

DIGITAL VIDEO EXPERTS

www.vitecmm.com

MEX tm

Multi-Channel Video Platform for OEMs & DSP Developers

MEX tm is the ideal solution for video surveillance systems where multiple cameras are used (up to 16 on a single board).

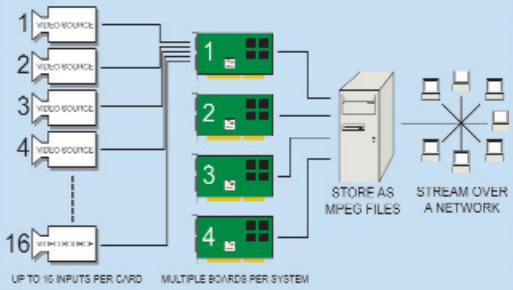
MEX™ is also well suited for video streaming over IP, digital video recorders and video servers.

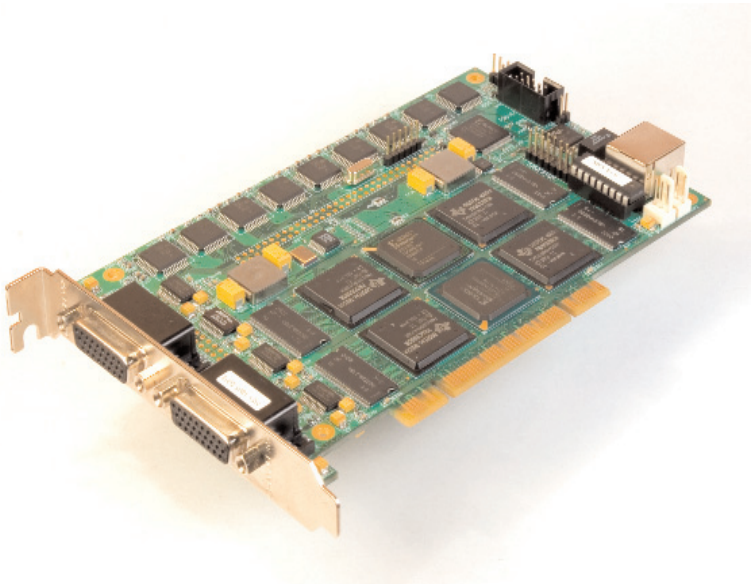
Each board is able to digitize 8 x 30 frames/second in NTSC and 8 x 25 fps in PAL/SECAM at full definition or 16 channels at reduced frame rate. Depending on the complexity of the codecs implemented in the four DSPs of the board, MEX can compress up to 8 x30 fps.

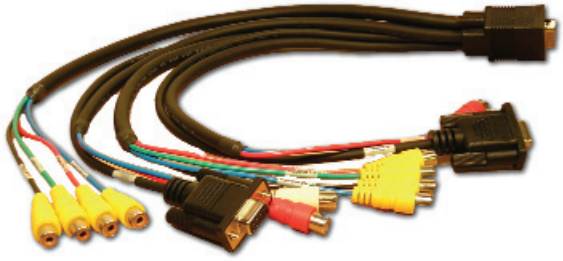
Key features :

- 19 GIPS and more,
- 4 x TMS320DM642™ DSPs,
- 16 x video inputs,
- 4 x stereo audio inputs,
- Audio and Video sync,
- Configurable architecture,
- Flexible codecs,
- 1 trigger input per channel,
- General Purpose IO per channel (1 input and 2 outputs),
- Ethernet interface,
- TCP/IP stack,
- PCI interface,
- Multi-board feature is supported,
- Standalone application (no PC).

TYPICAL SYSTEM SETUP AND OPERATION







VITEC MULTIMEDIA Inc. USA & Canada
2914 Seagull Drive – Duluth, GA 30096 - USA
Phone : (678) 580 3165
Fax : (678) 580 3295
Email : usa_info@vitecmm.com

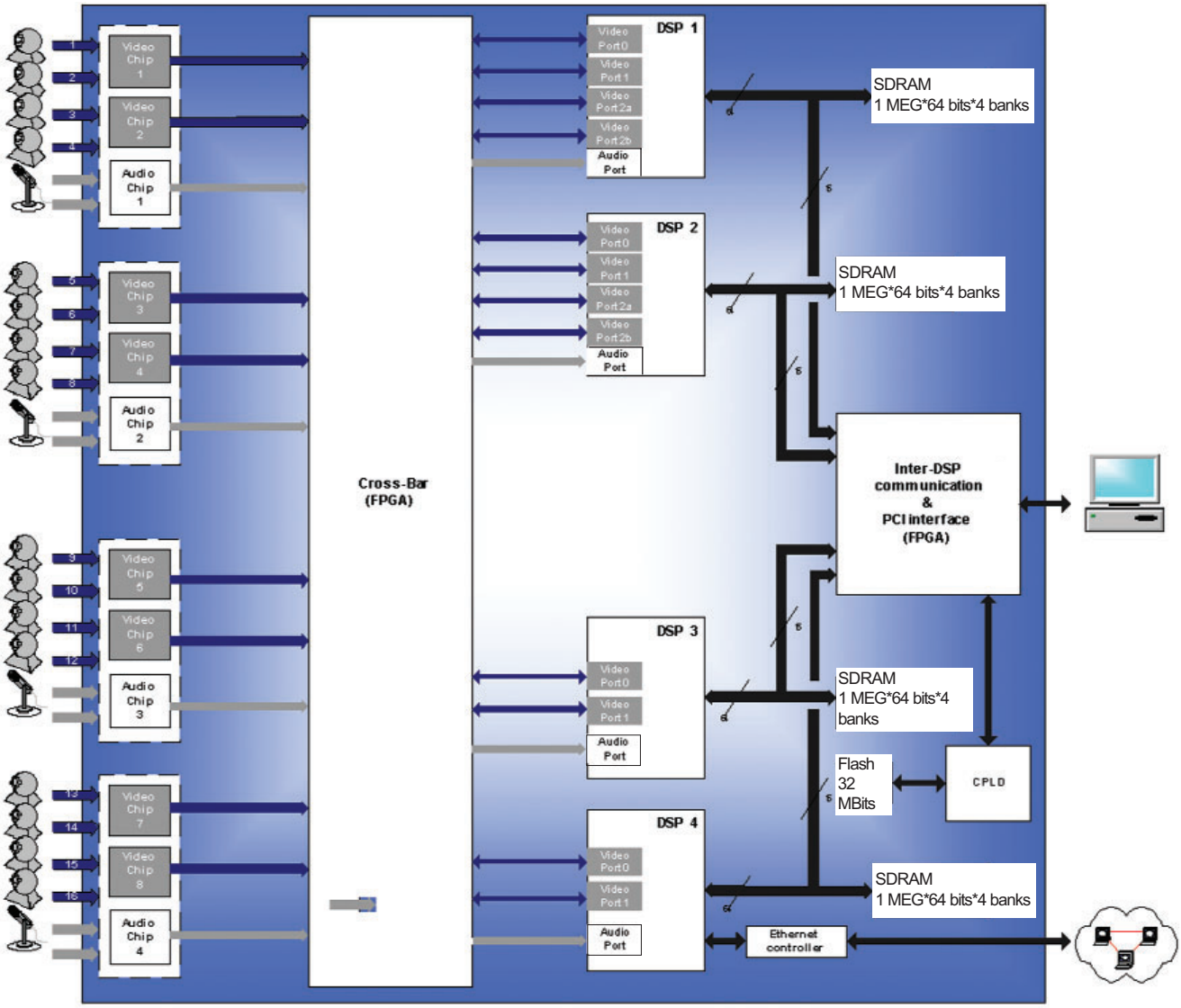
VITEC MULTIMEDIA International Sales
99, rue Pierre Sémard – 92324 Châtillon Cedex – France
Phone : +33 1 46 73 06 06
Fax +33 1 46 73 06 00
Email : info@vitecmm.com

ARCHITECTURE OF THE BOARD

The architecture of MEX™ includes 8 video decoders, 4 audio stereo ADCs, a crossbar, 4 DSPs, a PCI interface and a 100BaseT Ethernet controller. MEX also includes a 32 Mbits Flash memory which is used to store the microcode of the FPGA and DSPs especially in the standalone mode.

The DSPs are TMS320DM642™ from Texas Instruments running at 600 MHz or more (over 720 MHz in 05Q1) thus providing up to 19 GIPS with a maximum of 4 operations per instruction (4 operations of 8 bits, 2 operations of 16 bits and 1 operation of 32 bits) thus leading to a maximum of 76 GOPS.

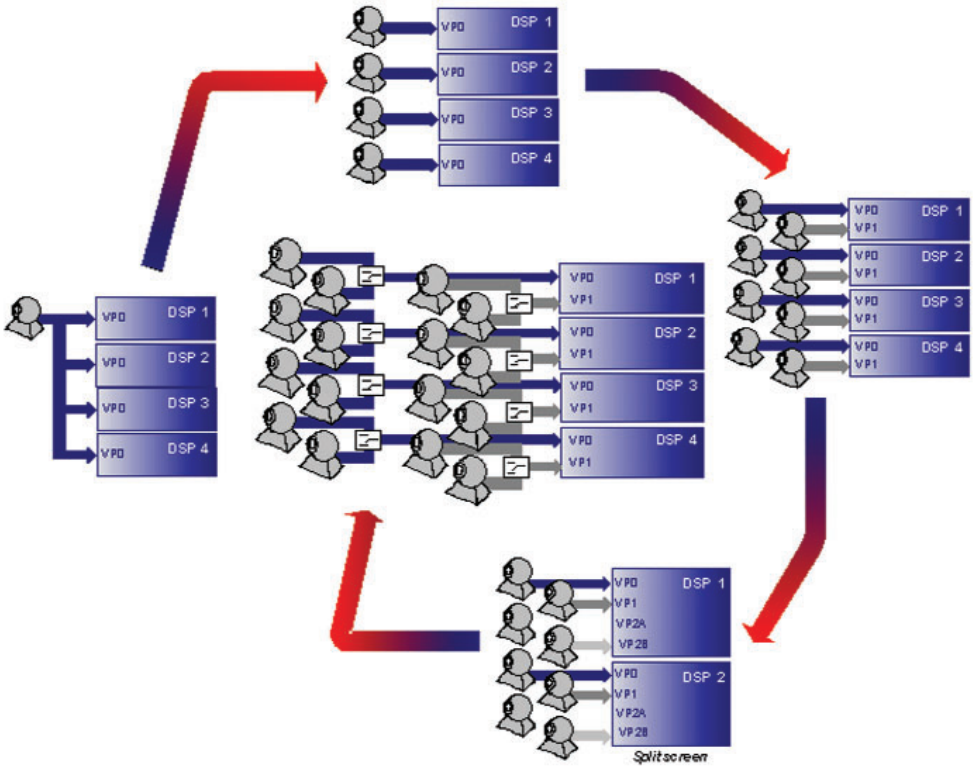
Each DSP has a private local memory of 32 MB (SDRAM running at 100 MHz and 64 bits, which provides a throughput of 800 MB/s).



CONFIGURABLE TOPOLOGY

Thanks to the cross-bar (implemented in an FPGA) and the multiple video ports of the DSPs, MEX™ has a highly flexible architecture. Typical examples of configuration include :

- 1 video source processed by 4 DSP to generate 4 different MPEG streams from the same content,
- 4 distinct video sources on 4 DSP,
- 8 distinct video sources on 4 DSP : 2 video per DSP on VP0 & VP1,
- 4 distinct video sources on 1 DSP (for split screen) : available on DSP1 and DSP2 > 2 split screen may be implemented,
- 16 distinct video sources on 4 DSP : by multiplexing video sources in the cross-bar. As a result, video frame rate will be reduced.



INTER-PROCESSORS COMMUNICATION

DSPs can communicate information to each others thanks to the "Inter-DSP communication & PCI interface" FPGA.

Each DSPs has a dedicated FIFO inside the FPGA which is mapped in its memory space. This FIFO can we written by the DSP and sent to :

- the host through the PCI interface,
- one or more other DSPs simultaneously through their own FIFO (multicasting).

The inter-DSPs communication means allow to use two or more DSPs to implement a single complex codec if required.

SOFTWARE TOOLS

MEX[tm] comes with a complete software environment :

- Windows WDM driver (.SYS),
- The source code of a sample application running under Windows XP/2000 and addressing directly the WDM driver,
- Source code of DSP sample applications such as :
  - video capture,
  - audio capture,
  - memory BIST,
  - DMA transfers.
- Vitec recommends the use of the Texas Instruments development tools to develop software for the DSPs themselves,
  - C/C++ compiler,
  - simulator,
  - emulator via the RTDS protocol and standard JTAG connector,
- Multi-DSP applications can be emulated by instancing several times the TI emulator software under Windows and the JTAG connector on the MEX[tm] board.

SOFTWARE TOOLS

A complete framework, called LiveWire™, for developers who want to use MEX™ hardware to develop a product running under Windows. LiveWire™ provides a set of ready to use connectable components leading to a drastic cut of the development time. LiveWire™ has many advantages. It :

- ensures highly flexible, scalable, truly customizable solutions,
- is designed to allow well-structured parallel development,
- allows to concentrate on solution specific tasks,
- overcomes the limitations of existing technologies such as DirectShow and COM in general,
- allows live reconnection of functional components without interruption of active processes,
- is compatible with Win32, COM, scriptable languages (Visual Basic, Java Script,...),
- takes advantages of XML based technologies and uses the Apache Xerces XML parser,
- provides different levels of SDK abstraction, from high level API for scripting languages through Win32 API for limited backward compatibility to the low level set of COM Interfaces for advanced development in C++.

LiveWire™ parts :
- LiveWire Core
- LiveWire Components
- LiveWire XML-based Profiles
- LiveWire Custom Components Wizard for MS Visual Studio C++
- LiveWire Multiplatform Shell
- LiveWire SDK
- LiveWire Tutorial and Samples

To start using LiveWire™ based products, all you have to do is to create an instance of Assembly Container, initialize it with XML-based Configuration Profile and run. Different sophisticated profiles can be created without extensive programming, using Integrated Property Page or directly by editing the XML file in the text editor of your choice. Components parameters persistence comes then automatically.

Very little programming is needed to use advanced features, such as Command Scheduling and Atomic Command Blocks. With a few extra lines of code you can complete an application capable of running execution scripts with frame accurate precision.

Custom LiveWire™ components creation is simplified by Wizard and they can be easily integrated into existing Assemblies.

The most important advantage of the SDK is the layered structure of the LiveWire™ framework which allows a quick development cycle.

TECHNICAL SPECIFICATIONS

Inputs	**Video formats :** NTSC, PAL, SECAM
	Video Inputs : 8 composite or 8 S-Video (Y/C) at full frame rate and resolution or 16 at reduced frame rate
	Audio inputs : 4 stereo or 8 mono
	GPIO : 8 inputs + 8 outputs with maskable vectorized interrupt
Digitization	**Video : each video input can be digitized at 720x480x30fps or 720x576x25fps in 4:2:2 sampling**
	Audio : the sampling rate of the audio inputs can be 32, 44.1, 48 KHz and the samples have a dynamic of 16 bits
Outputs	**Video and audio compression : the compression features are defined by the software codecs that the developer decides to implement in the DSPs. Many codecs can be found on the market at competitive prices. Check the TI's 3rd party software website**
	Outputs : Ethernet : 10 Base-T or 100 Base-TX Ethernet using single RJ-45 connector
Other features	Adjustments : brightness, contrast, saturation and hue as well as audio level for each channel separately
	Size : 175*107mm (6.875*4.2 inch)
	Weight : 155 g
	PCI interface : 32 bits 33 MHz PCI rev2.3 compatible with 5V and 3.3V (automatic detection)
	JTAG : 14-pin connector for external emulation hardware support. This is used to connect MEX™ to the TI emulator
	Autonomy : MEX™ can be used as a PCI plug-in card or as a **stand-alone equipment** with an external power supply (+5V and +3V) and a large Flash memory (32 Mbits) to store the DSP and the FPGA contents

DSPs SPECIFICATIONS

MEX™ uses 4 DSP DM642 :

- High-Performance Digital Media Processor :
  - 600-MHz Clock Rate
  - Eight 32-Bit Instructions/Cycle
  - 4800 MIPS
  - Fully Software-Compatible With C64x
- VelociTI.2. Extensions to VelociTI. Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x. DSP Core :
  - Eight Highly Independent Functional Units With VelociTI.2. Extensions:
  - Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle
  - Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle
  - Load-Store Architecture With Non-Aligned Support
  - 64 32-Bit General-Purpose Registers
  - Instruction Packing Reduces Code Size
  - All Instructions Conditional
- Instruction Set Features
  - Byte-Addressable (8-/16-/32-/64-Bit Data)µ
  - 8-Bit Overflow Protection
  - Bit-Field Extract, Set, Clear
  - Normalization, Saturation, Bit-Counting
  - VelociTI.2. Increased Orthogonality
- L1/L2 Memory Architecture
  - 128K-Bit (16K-Byte) L1P Program Cache (Direct Mapped)
  - 128K-Bit (16K-Byte) L1D Data Cache (2-Way Set-Associative)
  - 2M-Bit (256K-Byte) L2 Unified Mapped RAM/Cache (Flexible RAM/Cache Allocation)
- Endianess: Little Endian
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- 10/100 Mb/s Ethernet MAC (EMAC)
- Three Configurable Video Ports : supports Multiple Resolutions and Video Standards
- Three 32-Bit General-Purpose Timers
- IEEE-1149.1 (JTAG†)

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.